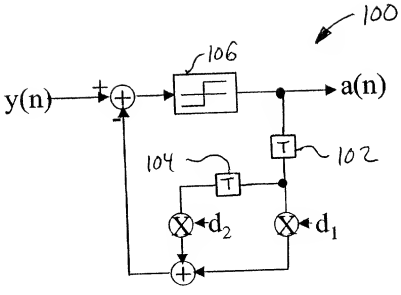


FIG. 1

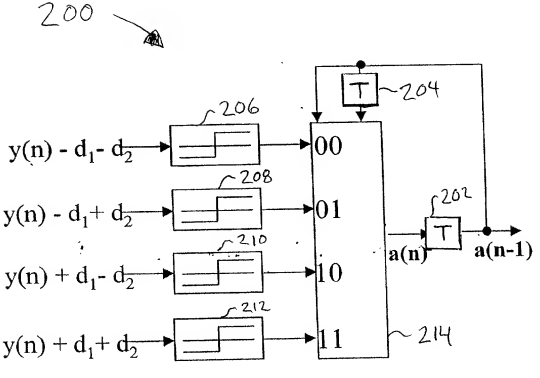


FIG. 2

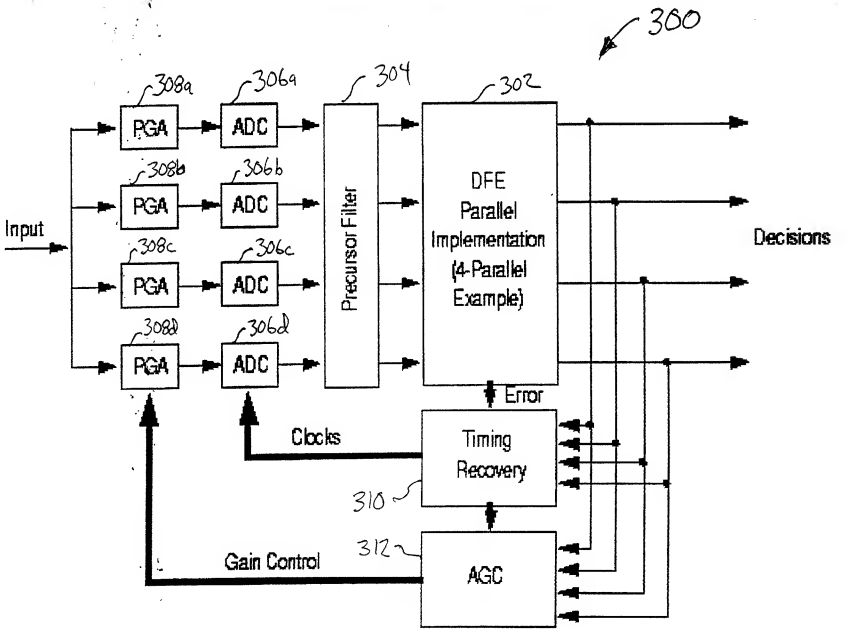


FIG. 3

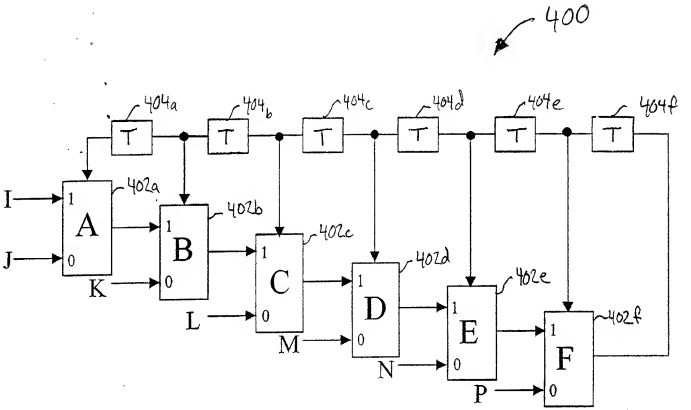


FIG. 4

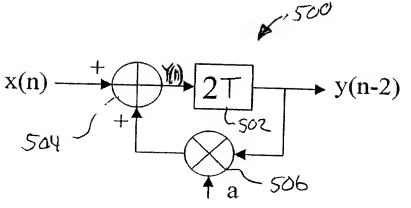


FIG. 5

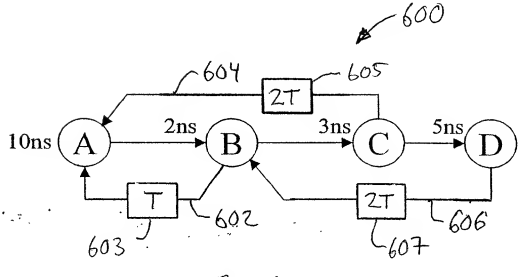


FIG. 6

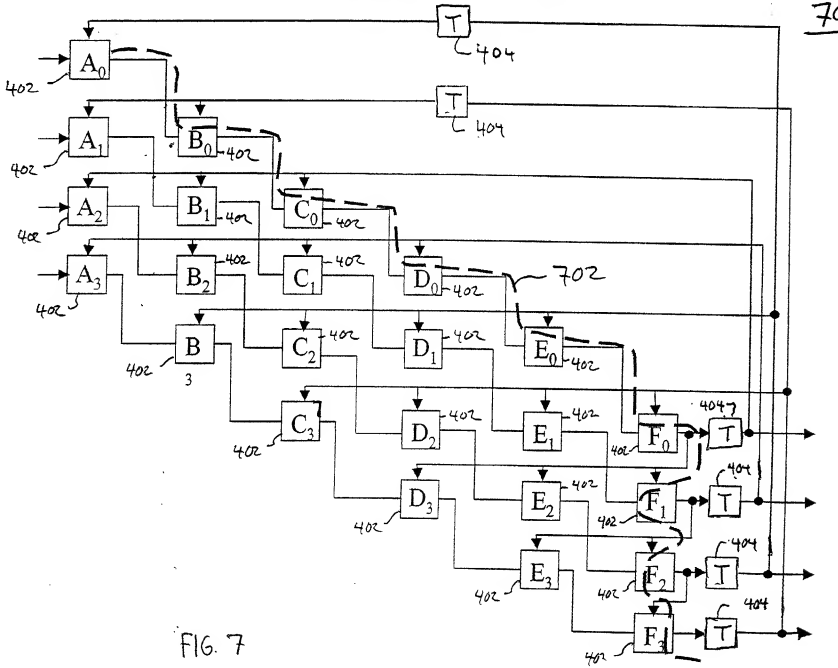


FIG. 7

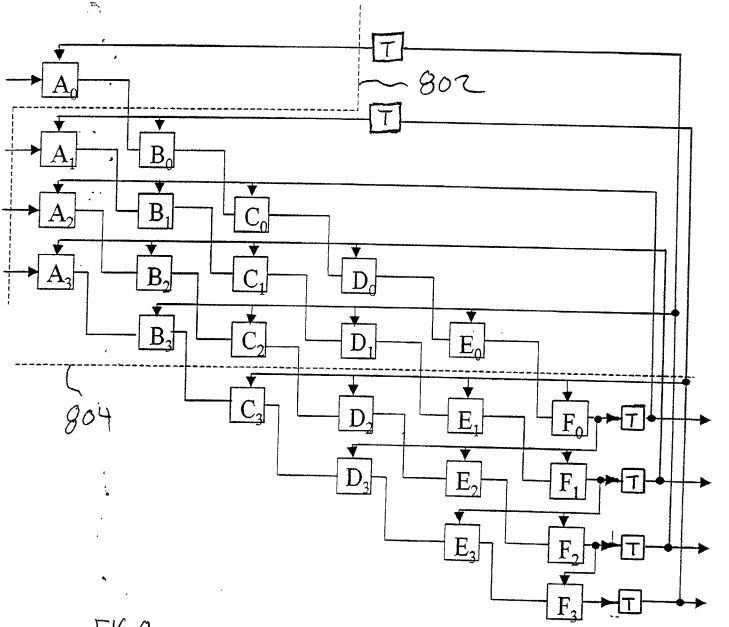


FIG. 8

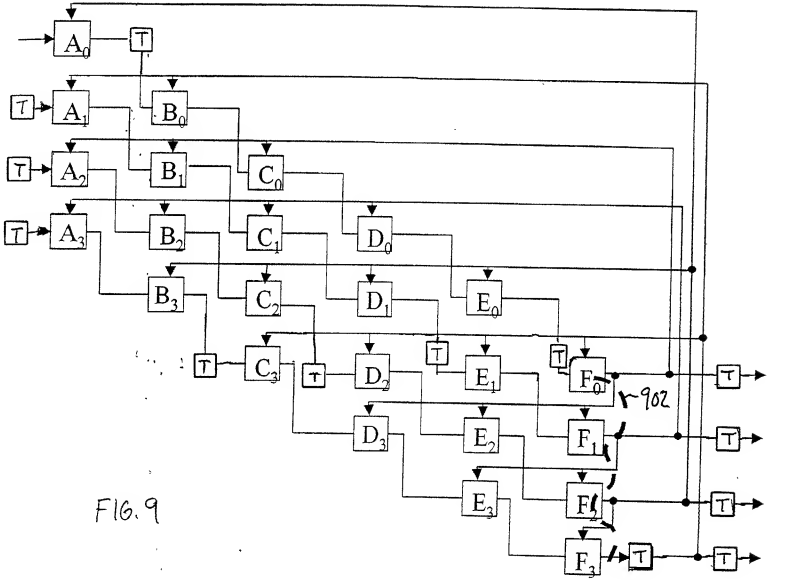


FIG. 9

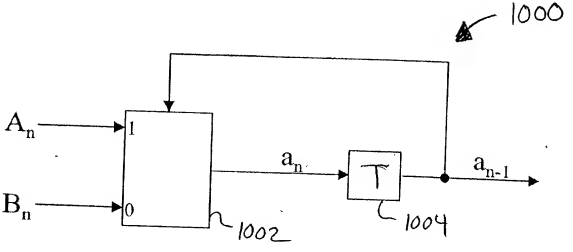


FIG. 10

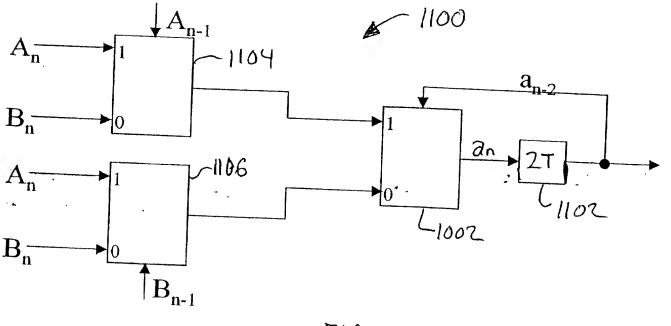
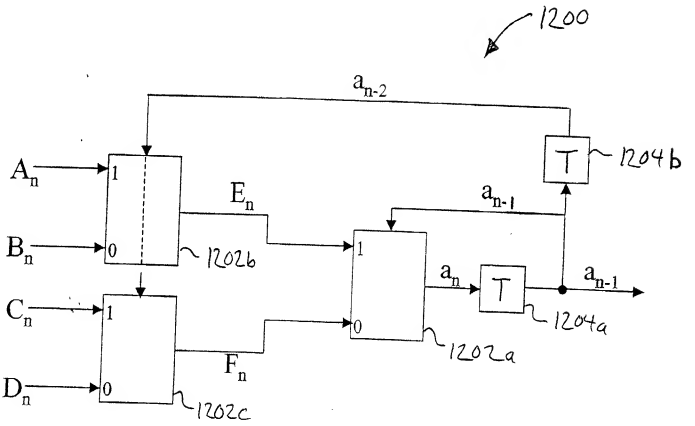


FIG. 11



F16. 12

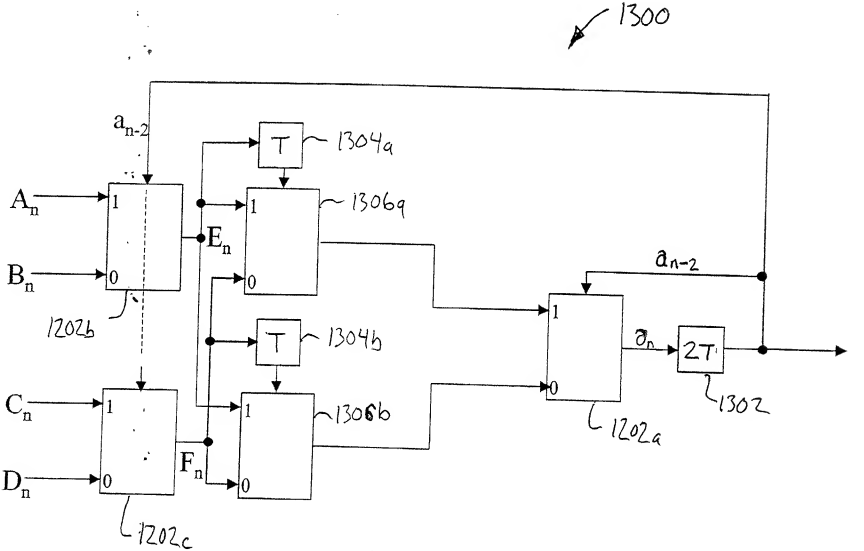


FIG. 13

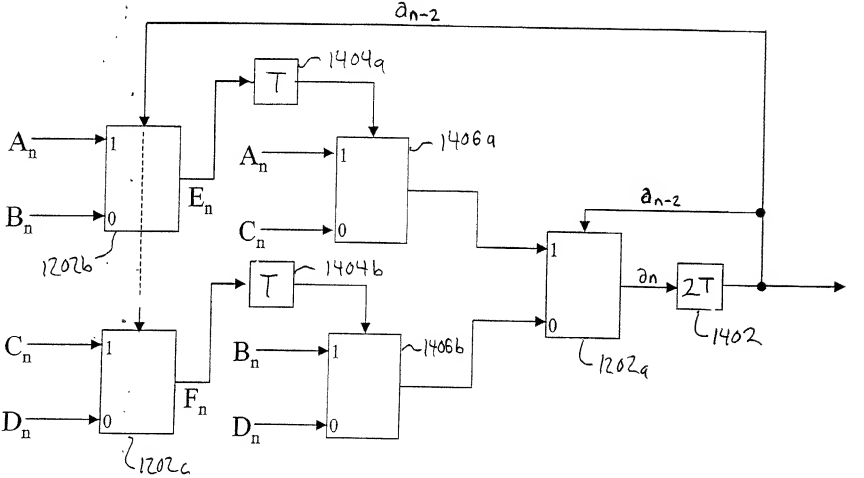
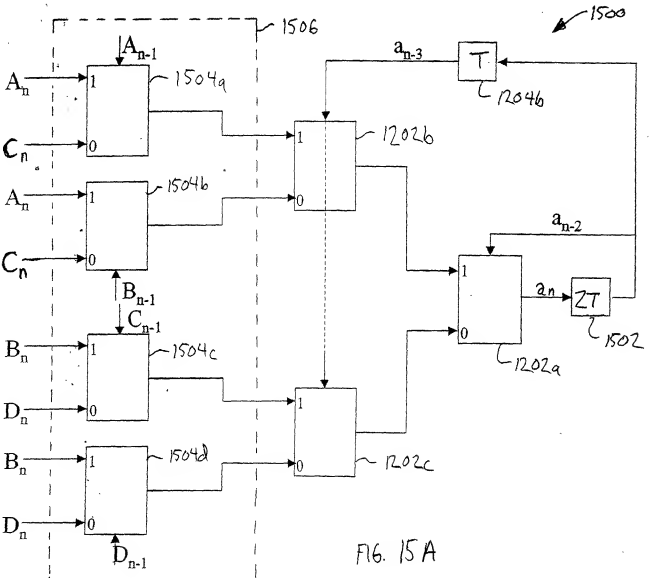


FIG. 14


1500
1506
A_{n-1}
A_n
1504a
C_n
1202b
a_{n-3}
T
1204b
A_n
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C_n
a_{n-2}
B_{n-1}
C_{n-1}
a_n
ZT
1502
B_n
1504c
D_n
1202a
B_n
1504d
1202c
D_n
D_{n-1}

FIG. 15A

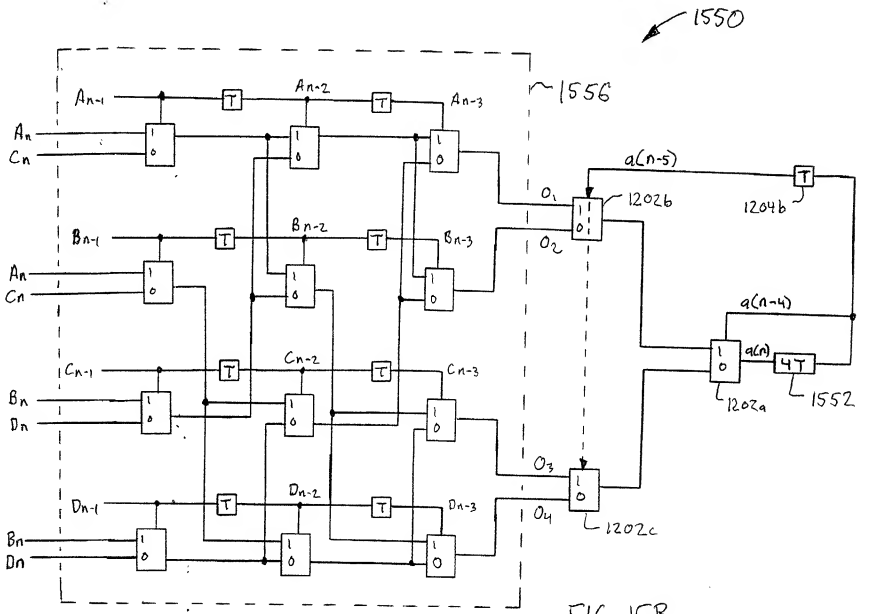


FIG. 15B

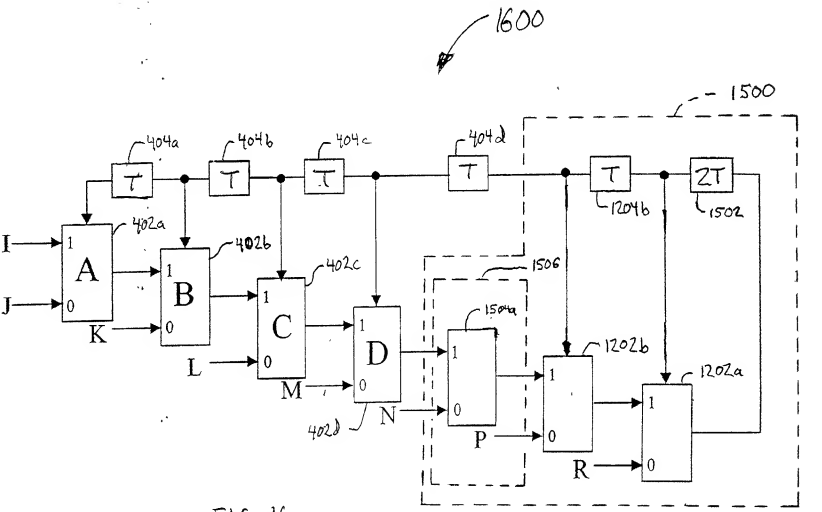
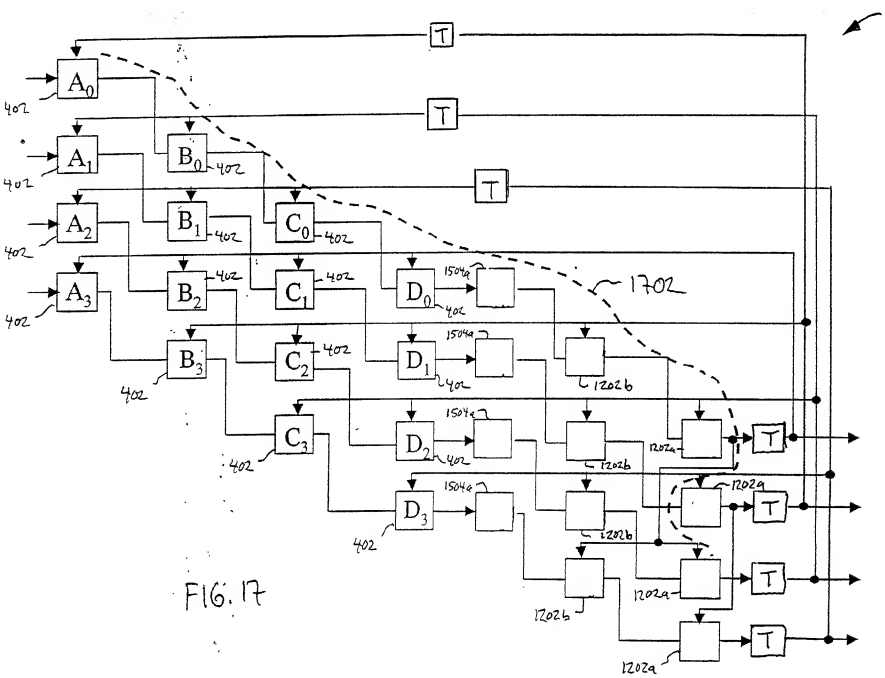


FIG. 16



F16. 17

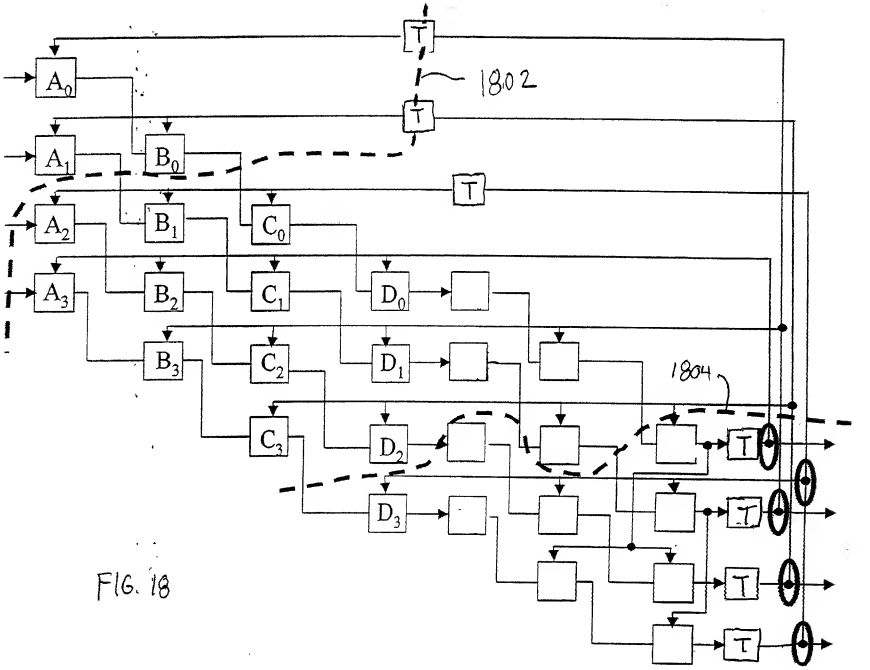


FIG. 18

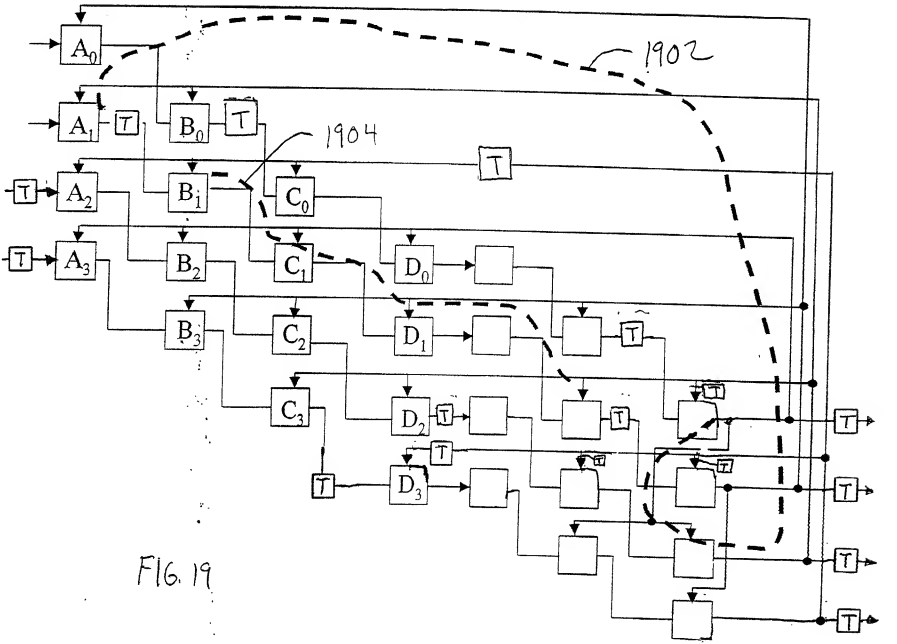


FIG. 19

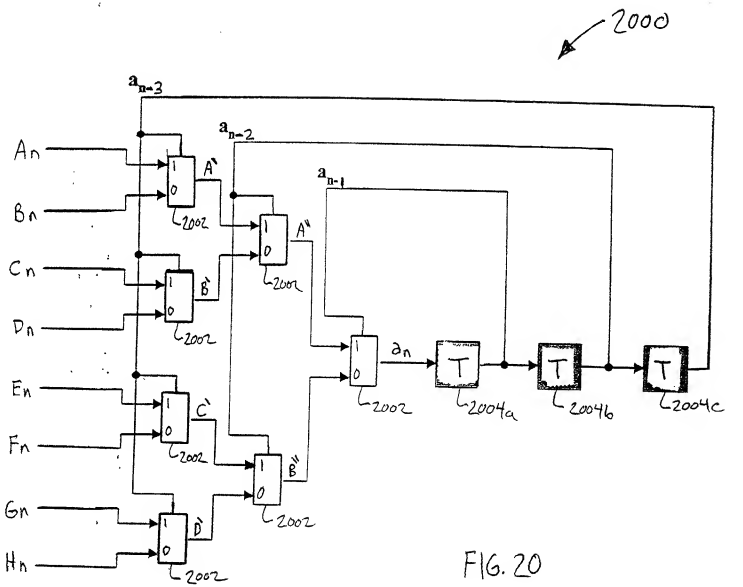


FIG. 20

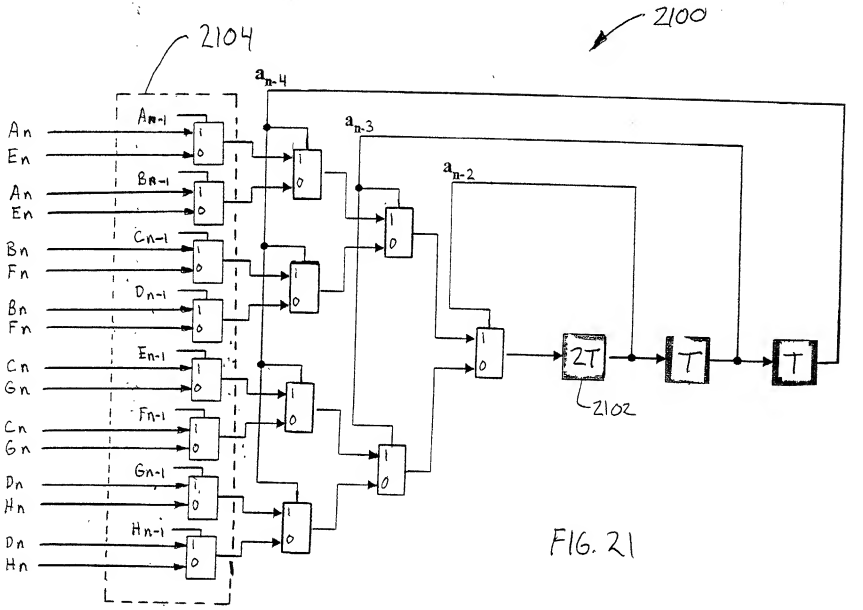


FIG. 21

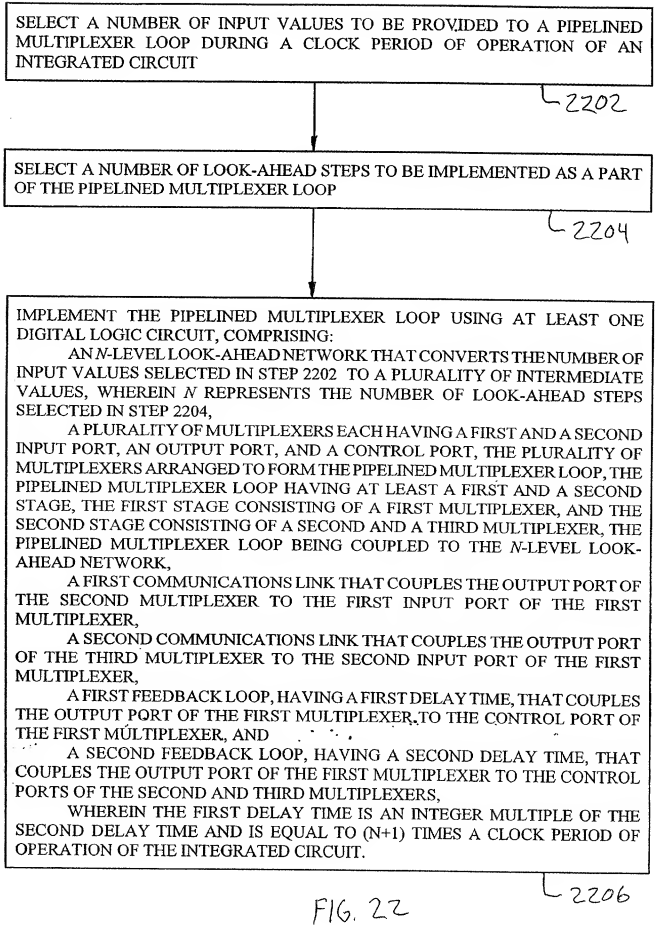


FIG. 22

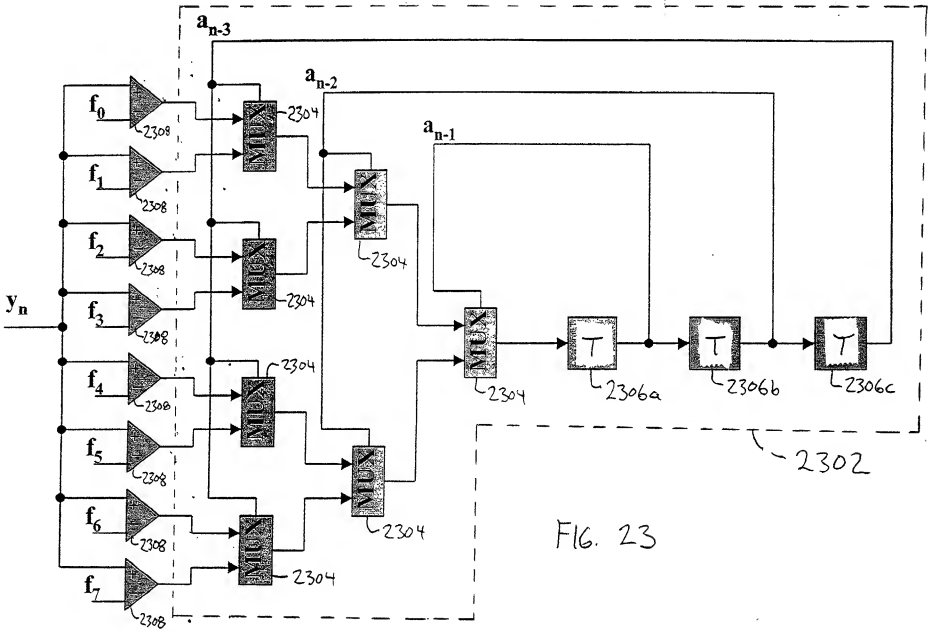


FIG. 23

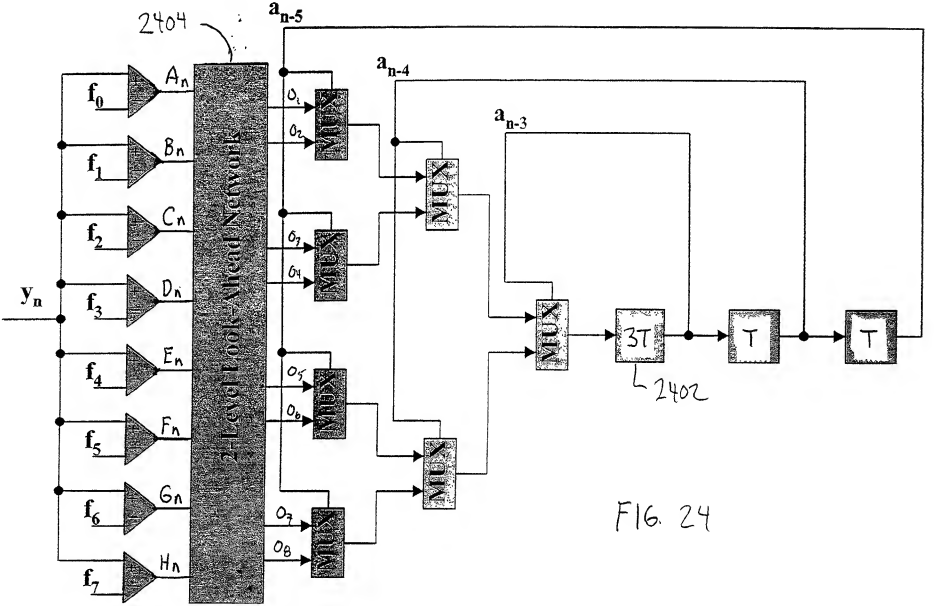


FIG. 24

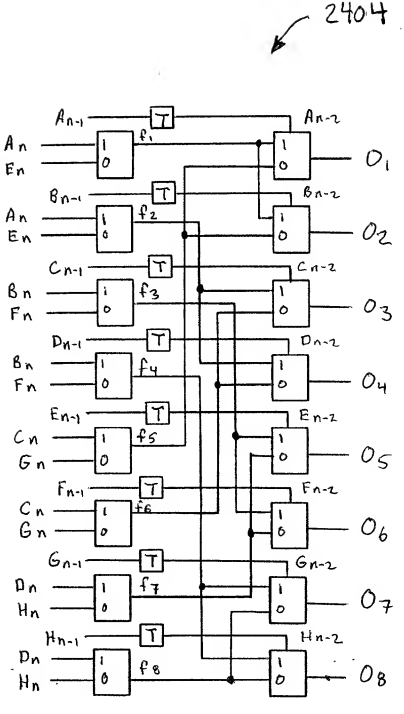


FIG. 25

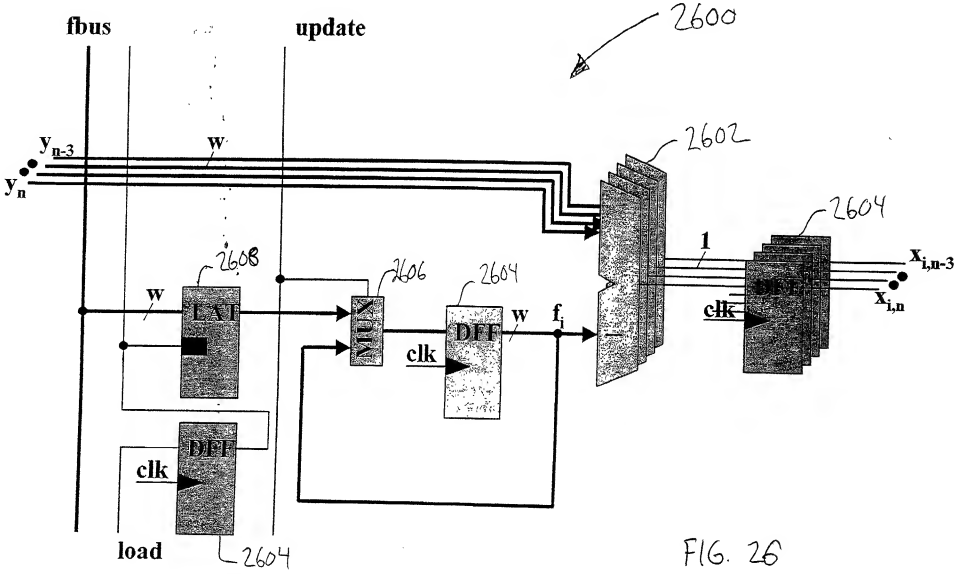


FIG. 26

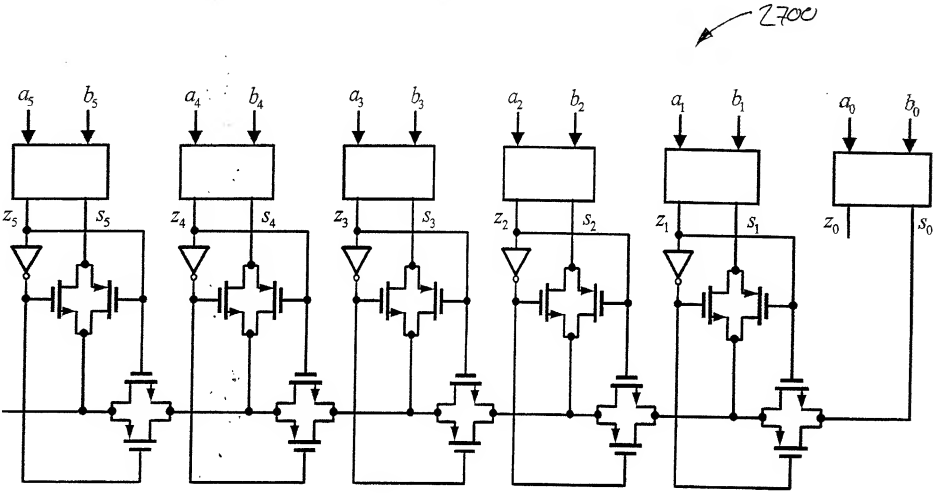
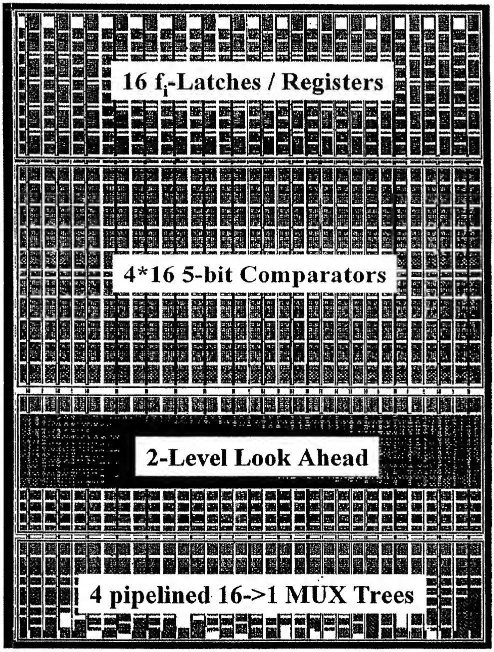


FIG. 27


16 f_i-Latches / Registers
4*16 5-bit Comparators
2-Level Look Ahead
4 pipelined 16->1 MUX Trees

2800

FIG. 28